AMENDMENTS TO THE DRAWINGS

The attached "Replacement Sheet(s)" of drawings includes changes to Figure 1. The attached "Replacement Sheet(s)," which includes Figure 1, replaces the original sheet including Figure 1.

Attachment: Replacement Sheet(s)

REMARKS

Claims 43-48, 51-67 and 70-88 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

DRAWINGS

The drawings stand objected to for certain informalities. Applicant has attached a revised drawing for the Examiner's approval. In the "Replacement Sheet", Figure 1 has been amended to define boundaries for each column that defines a neuron. The amendment is readily understood by one skilled in the art in view of the teachings of the specification as originally filed, including paragraph [0026]. Therefore, reconsideration and withdrawal of this objection is respectfully requested

REJECTION UNDER 35 U.S.C. § 112

Claims 49, 68 and 89 stand rejected under 35 U.S.C. § 112, first paragraph, a failing to comply with the written description. This rejection is respectfully traversed. Given the teaching of the present application, one skilled in the art would readily understand how interconnects in Figure 1 could be rearranged, such that each row (as opposed to column) corresponds to a neuron. Rather than amend the specification, applicant elects to delete these claims from the application, thereby rendering the rejection moot. However, such a configuration is considered to fall within the scope of other remaining claims. Therefore, reconsideration and withdrawal of this rejection is respectfully requested

REJECTION UNDER 35 U.S.C. § 101

Claims 43-90 stand rejected under 35 U.S.C. §101 for being nonstatutory subject matter. This rejection is respectfully traversed.

Applicant's invention is directed generally to an architecture for a chip and thus falls within one of the four statutory categories (i.e., a machine). On the contrary, the Examiner asserts that the claims are directed to an abstract concept of a chip that is self programming. The Examiner errs by focusing only upon the preamble of the claim when formulating this rejection. The body of the pending claims clearly recite an array of cells which form a network and a particular arrangement for each cell which includes multipliers, capacitors and digital memory. These circuit components are neither an abstract idea, a law of nature, nor a natural phenomena. Therefore, the pending claims do not fall within a judicial exception to statutory subject matter. As a result, there is no need for the pending claims to recite a practical application. Accordingly, applicants respectfully request the Examiner to reconsider and withdraw this rejection.

The Examiner's attention is also draw to Claim 62 which does recite a practical application. For this additional reason, reconsideration and withdrawal of this rejection in relation to this claim is respectfully requested.

REJECTION UNDER 35 U.S.C. § 102

Claims 43-57, 59-76 and 78-80 stand rejected under 35 U.S.C. §102(b) as being unpatentable over a dissertation by Oh entitled "Analog CMOS Implementation of Artificial Neural Networks for Temporal Signal Learning" (Oh). This rejection is respectfully traversed.

Applicant's invention is directed generally to a self-programmable chip. Of note, Claim 44 recites that each synaptic cell in an array of synaptic cells stores weights for the cell locally in a capacitor and locally in a digital memory. Independent claims 62 and 81 recite similar subject matter. In contrast, Oh teaches that the capacitor for storing a weight is located outside an array structure as described on page 126, lines 3-9 of the dissertation. For at least this reason, we feel that the pending claims are patentably distinct from the relied upon reference.

The Examiner also relies on page 116, lines 2-17 of the dissertation to reject the pending claims. However, the Examiner has misinterpreted the teachings of this portion of the reference. For instance, this section does not describe an array architecture as recited in the pending claims, but rather discusses the general/generic approach on how to possibly refresh the weights. It does not detail how the interface is manifested or how many weights for that matter. It does not discuss timing issues or organization. It describes the costly process of possibly reading the weight values via an externally interface(s), with an A/D, then storing the weights on an external digital form, then refreshing the weights by an interface circuitry and D/A. It does not concern itself with how long this would take, how may weights it can handle, how the signal internally in the chip is routed or switched from one weight to the other. On the face of it, it simply refers to this potential approach, and then it discards it in favor of the approach it describes in the second paragraph (see Oh, p 116:11-17).

This approach of storing the weights off-chip has may known limitations. e.g.,: (1) expensive discrete (not integrated) components, (2) does not preserve the weight value due to signal transfers along "long" wires inside and outside the chip (losses), (3)

increase of noise and low SNR, (4) complexity of interface wiring inside and outside the chip to route the weight signal values from a specific location of the weight array to a single external A/D and D/A interface circuitry, (5) a non self-contained processing solution that always requires the interface to the external computing platform (e.g., a PC). Oh, then states that this approach will be expensive and thus proceeds to the approach in the second paragraph of this section (Section 5.6.4, Oh, p116:11-17) whereby one uses a duplicate (master) neural network to exclusively focus on the learning process and a slave network that uses a copy of the learned weights to maintain the weights as long as learning is on going. For these additional reasons, we feel that the teachings of the Oh reference are deficient as applied to the pending claims. Accordingly, Applicants respectfully request the Examiner reconsider and withdraw these rejections.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested.

If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: June 27, 2007

By: _____
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